Millimeter-Wave Characteristics of Flip-Chip Interconnects for Multichip Modules

Wolfgang Heinrich, Andrea Jentzsch, and Guido Baumann

***Abstract*— Electromagnetic simulation and measurement data of flip-chip transitions are presented. First-order effects are identified and design criteria for millimeter-wave multichip interconnects are derived. Results cover chip detuning and bump geometry as well as simplified modeling. In a coplanar environment, the flip-chip scheme provides interconnects with excellent low-reflective properties. For conductor-backed structures, parasitic modes occur leading to unwanted crosstalk. These effects dominate the behavior so that overall performance of the flip-chip scheme can be evaluated properly only in conjunction with the actual motherboard packaging setup.**

***Index Terms*— Finite-difference methods, flip-chip devices, MMIC multichip modules, packaging.**

I. Introduction

COST-EFFECTIVE packaging is a precondition for the development of commercial millimeter-wave (mm-wave) systems. Among the multichip module schemes available, the flip-chip approach is one of the most promising ones. For single chips, excellent mm-wave properties have been demonstrated [1]–[3]. It is not clear, however, whether these results can be generalized to more complex systems and which are the design criteria. Electromagnetic modeling of flip-chip interconnects has been the subject of several publications (e.g., [4]–[6]), but a comprehensive treatment of the electromagnetic behavior in view of the practical limitations is still missing. This is the motivation for this paper.

The purpose is to provide guidelines to the design engineer what determines the mm-wave characteristics of flip-chip interconnects, how they should be designed from an electromagnetic point of view, and what are suitable modeling tools for practical system development.

The results presented in this paper are based on extensive simulations using a three-dimensional (3-D) finite-difference frequency-domain (FDFD) code developed from [7] and backed by measurements of test structures.

II. Chip Detuning and Bump Height

The first important parasitic effect introduced by flip-chip mounting is detuning of the chip. Due to flipping, the surface of the motherboard is near to the elements on the chip surface with the distance being approximately the bump height. This changes the electrical characteristics of the on-chip elements, which are especially pronounced for transmission lines. One has to distinguish whether or not a metallization is present on the motherboard below the chip. Fig. 1 illustrates the resulting deviations for a typical coplanar waveguide with 50-μm ground-to-ground spacing on GaAs.

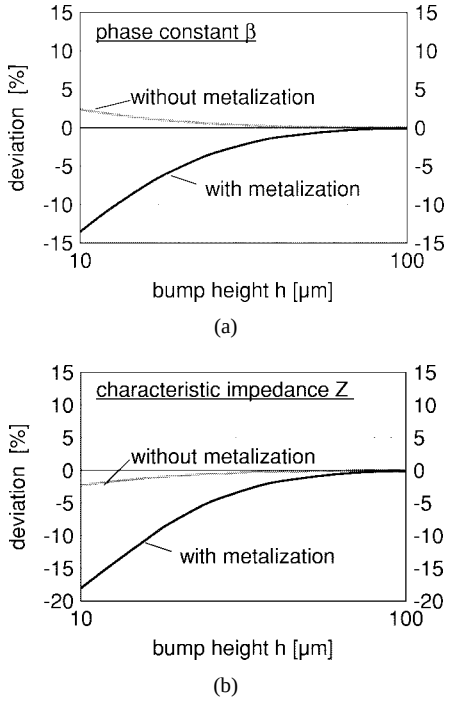

Fig. 1. Deviations of CPW transmission-line parameters as a function of flip-chip bump height h for the case with and without metallization on the surface of the motherboard below the chip (50-Ω CPW with 50-μm ground-to-ground spacing on GaAs). (a) Phase constant β. real (b) part of characteristic impedance Z.

From the data in Fig. 1, one concludes that any metallization underneath the flipped chip has a significant influence. For the nonmetallized case, bump heights in the order of 20 μm lead to deviations below 2%, which usually can be tolerated. Using a metallized motherboard surface, however, one requires considerably larger heights in order to prevent severe detuning. Then, for technological reasons, the bump cross-sectional dimensions have to be increased accordingly since the bump aspect ratio is fixed. As a consequence, pad size grows as well and high-frequency performance deteriorates. The data in Fig. 1 refer to a 50-μm-wide coplanar waveguide (CPW) on the chip. When increasing ground-to-ground spacing or

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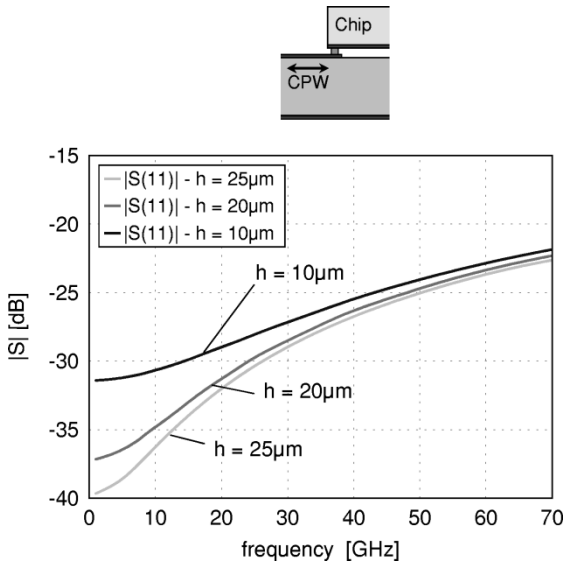

Fig. 2. Reflection coefficient of a single flip-chip transition as a function of frequency with the bump height h as a parameter (50-Ω CPW with 120-μm ground-to-ground spacing on motherboard and chip, bump cross section is 25 $\times$ 25 μm^2).

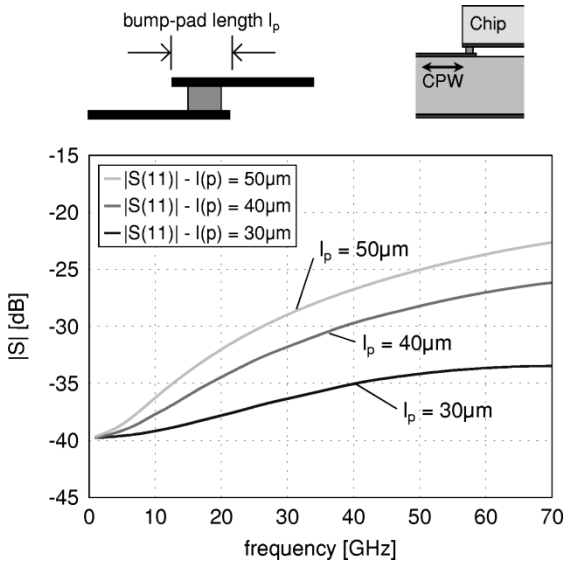

Fig. 3. Reflection coefficient of a single flip-chip transition against frequency with the bump-pad length l_p as the parameter (l_p denotes the bump-pad dimension in the propagation direction; bump height and width are both 25 μm, with the rest of the data as in Fig. 2).

when using microstrip lines instead of CPW, one obtains even larger deviations. Of course, a defined detuning can be taken into account already in circuit design. But this requires special modeling tools and chip measurement setups. Hence, from the electromagnetic point of view, the nonmetallized case shows clear advantages.

III. Reflection of Coplanar Mode at the Interconnect

In this section, a single transition from a CPW line on the motherboard to a CPW line on the flipped chip is considered. The question is how bump geometry influences the reflection of the transition. Figs. 2 and 3 present 3-D electromagnetic

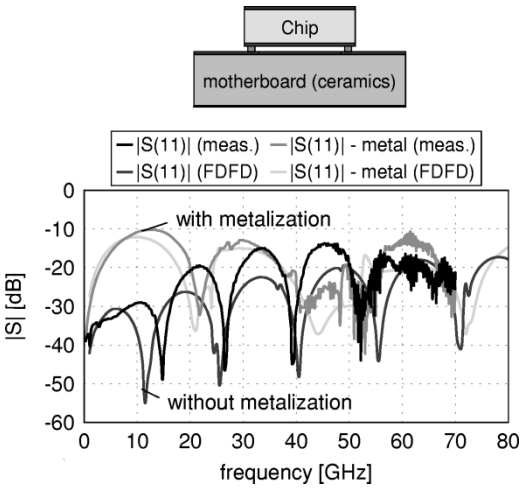

Fig. 4. Reflection due to flip-chip mounting against frequency: measurement and FDFD simulation data for the cases with and without metallization on the motherboard surface below the chip. The chip contains a CPW through-line (bump height $h = 25$ μm, chip length 4.2 mm, and the rest of the data as in Fig. 2).

simulation results. In Fig. 2, the parameter is bump height h; in Fig. 3, bump-pad length l_p (i.e., the bump-pad dimension in the propagation direction) is varied.

The unexpected finding is that bump-pad length is the most important parameter in the mm-wave frequency range while bump height does not influence reflection significantly (the differences at lower frequencies are caused by detuning effects mentioned above and not by parasitics of the transition itself). Further investigations reveal that the transition shows a capacitive behavior and not an inductive one, as might be expected when describing the bump section by a three-conductor line in air (e.g., [5]). The cross section of the bump (circular, elliptic, or rectangular shape), on the other hand, is of minor influence.

Quantitatively, the return loss data in Figs. 2 and 3 are excellent and demonstrate the potential of the flip-chip technique for mm-wave applications. When evaluating practical relevance, however, the transitions have to be considered together with the motherboard packaging scheme, as explained in Section IV.

IV. Parasitic Modes

A. General Considerations

Besides the reflection of the CPW mode at the interconnect, the existence of parasitic substrate modes in the motherboard must be accounted for. For the flip-chip scheme, mainly two types of parasitic modes are relevant.

- When using a metallized motherboard surface below the chip, an additional parallel-plate mode exists in the air region between the two substrates (see also [6]). This causes parasitic coupling and half-wavelength resonances. In Fig. 4, measurement and simulation results for a test structure are given. As expected, one observes parasitic resonances, which cause reflection coefficient values of -10 dB already at 10 GHz.

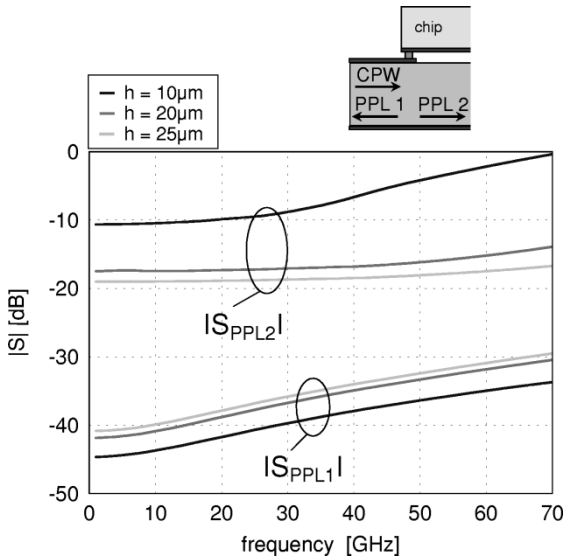

Fig. 5. Transmission into parasitic PPL modes at a single flip-chip transition with bump height h as the parameter (for mode definition see inset, and the other data are as in Fig. 2).

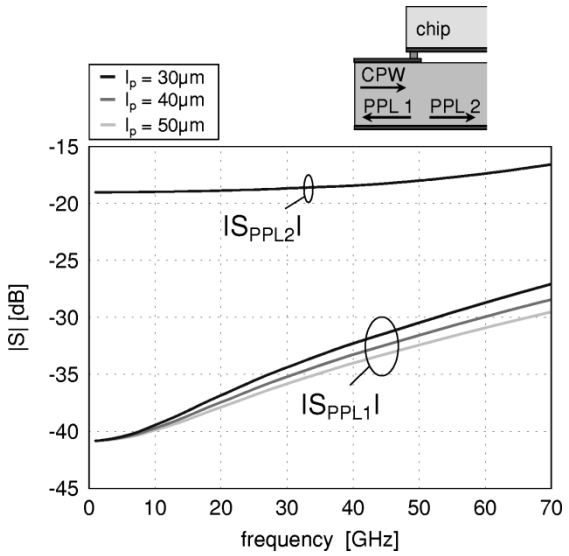

Fig. 6. Transmission into parasitic PPL modes at a single flip-chip transition with bump-pad length l_p as parameter; for S_{PPL2} the curves for $l_p = 30 \cdots 50$ μm coincide (for mode definition see inset, with the rest of the data as in Fig. 3).

- In common packaging setups, the backside of the motherboard is conducting. The conductor is formed either by the backside metallization or by the bottom plane of the package. Therefore, in both cases, a parasitic parallel-plate (PPL) mode is propagating in the motherboard. It couples to the desired CPW mode at any discontinuity, i.e., at bump interconnects as well as at package feedthroughs, etc. The results are parasitic paths that reduce isolation between ports (see also [6], [8]), which may cause severe circuit instabilities. This situation is treated in more detail in Section IV-B.

B. The Conductor-Backed Case

First, a single interconnect is studied (see the inset of Fig. 5). Due to the existence of the PPL modes, a part of the incoming CPW signal is scattered at the bump interconnect into a forward and a backward PPL mode. In Fig. 5, the transmission coefficients into the two PPL modes are plotted with the bump height h as a parameter. Fig. 6 provides the corresponding curves for different bump-pad lengths. The most striking observation is that coupling to the PPL mode in forward direction (S_{PPL2}) is above -20 dB, which is larger than the CPW reflection (see Figs. 2 and 3). S_{PPL2} depends only on bump height h and shows a slight decrease with growing h.

A special effect should be noted in this regard. At a bump height of 10 μm, degeneracy phenomena occur for the given geometry, because the propagation constants of CPW and PPL mode in the chip section approach each other in a certain frequency range. This leads to coupling coefficients in excess of -5 dB. In its pure form, this effect is mainly of academic interest, but it indicates potential problems in practice if bump height is small and if the chip and motherboard substrates are of similar permittivity.

In contrast to S_{PPL2}, transmission into the backward PPL mode (S_{PPL1}) remains small with magnitude values below -30 dB and, therefore, can be neglected for most practical applications.

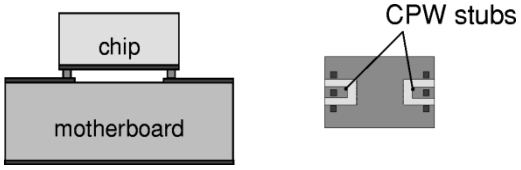

Fig. 7. Test structure for determining crosstalk: flipped chip with two opposite CPW open stubs (ideally, there should be no transmission).

What does PPL-mode coupling mean for multichip arrangements? In order to clarify this, the structure shown in Fig. 7 is treated. It contains a flipped chip with two opposite CPW open stubs. Ideally, i.e., without the PPL mode, transmission should be zero since the distance between the stubs is large so that CPW coupling vanishes. But, since the ground metallization connects both ports, the PPL mode can propagate in the entire motherboard. The edges of the motherboard present a highly reflective boundary to the PPL mode, which is described by the reflection coefficient r_{PPL} in the model of Fig. 8. The parameter r_{PPL} can be approximated by -1, i.e., a short circuit, if CPW ground and backside conductors are connected by the package, or by $+1$, i.e., an open, if there is no electrical connection nor radiation. In both cases, the motherboard forms a low-loss resonator for the PPL mode that is coupled to the CPW transmission lines at each bump interconnect. Fig. 8 demonstrates the result: parasitic crosstalk is observed between the CPW stubs with transmission peaks approaching 0 dB at certain frequencies.

In order to illustrate the influence of the PPL-mode resonance phenomena, the case $r = 0$ is plotted in Fig. 8 as well. This condition refers to an extremely low-quality resonator, i.e., power leaks away at the substrate edges. As a consequence, the peaks vanish almost completely, but nevertheless parasitic coupling in the order of -30 dB is

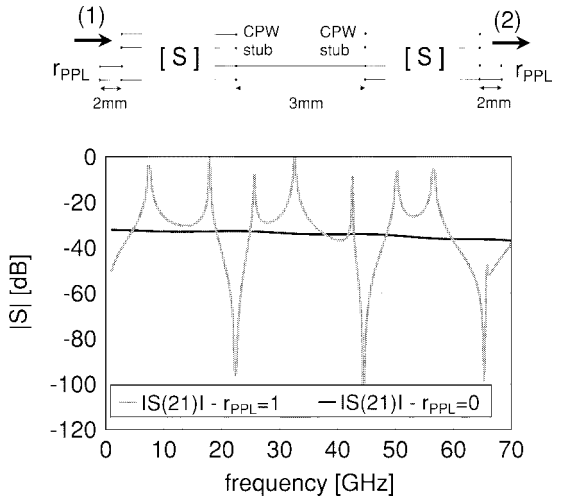

Fig. 8. Transmission between CPW stubs against frequency (test structure, see Fig. 7); the outer PPL ports are matched with reflection coefficient r_{PPL}. Total motherboard length: 2 mm + 3 mm + 2 mm = 7 mm.

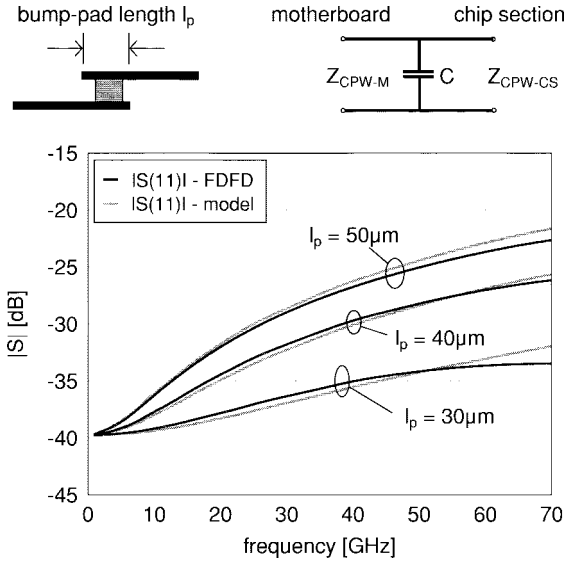

Fig. 9. Simple equivalent-circuit model of the flip-chip interconnect by using a single capacitance C (see inset): comparison to FDFD results in Fig. 3 (parameter: bump-pad length l_p). The other data are as in Fig. 3.

observed, which may be too large for modules with high-gain or low-crosstalk specifications. Summarizing, one can state that, in any conductor-backed setup, the parasitic PPL modes induce unwanted crosstalk between flip-chip bump interconnects, which limits maximum isolation to the −30-dB level and causes severe instability problems at motherboard resonances.

V. Simplified Modeling

Based on the FDFD simulations, simplified models for the flip-chip transition can be developed. Because of the high return loss, simple models yield sufficient accuracy for circuit design. For the CPW mode, the bump interconnect can be described by a lumped shunt capacitance C at the transition. In Fig. 9, this model is compared to the em simulation data for different bump-pad lengths (see Fig. 3). Despite the simple model, one obtains good accuracy. The capacitance C can be related to the stacking of the chip and the motherboard in the bump section. Thus, one has high-ε_r substrates both below and above the CPW conductors, which represents an excess capacitance. In this way, C can be approximated by means of closed-form expressions.

In order to determine parasitic-mode coupling S_{PPL2}, the method of [8] can be applied. Using this approach, one obtains accurate information without computationally expensive 3-D calculations. The magnitude of S_{PPL1}, on the other hand, is small so that it may be neglected in most applications.

VI. Conclusions

Electromagnetic simulation of the flip-chip transition yields some important design criteria for multichip module schemes.

- Metallization on the motherboard below the chip should be avoided. For common bump heights below 25 μm, it causes severe detuning and parasitic half-wavelength resonances.
- In a coplanar environment, the reflection characteristics of the bump structure itself are excellent up to the mm-wave range. The first-order parameter is the longitudinal dimension of the bump pad, not the bump height. The influence of the cross-sectional shape (rectangular, circular, or elliptical) is of minor importance and can be adapted to the fabrication process. For common bump and substrate geometries, the transition shows a capacitive behavior. A simplified description of the transition by a lumped capacitance yields good accuracy.
- Since in most practical multichip schemes one has a conducting backside, the key issue is not the bump interconnect itself but the motherboard packaging concept. Due to conductor-backing, the structure supports a parasitic mode with a volume-type field pattern between the backside and the CPW ground metallization. This mode gives rise to coupling and resonances between ports, especially in the mm-wave range, where chip dimensions exceed half the wavelength. Hence, when developing a unified approach for mm-wave MCM's, flip-chip mounting needs to be considered together with the motherboard packaging concept.

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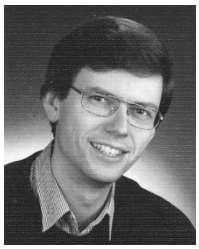

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